Application Note for 64Mb HyperRAM Chip ID Read Function

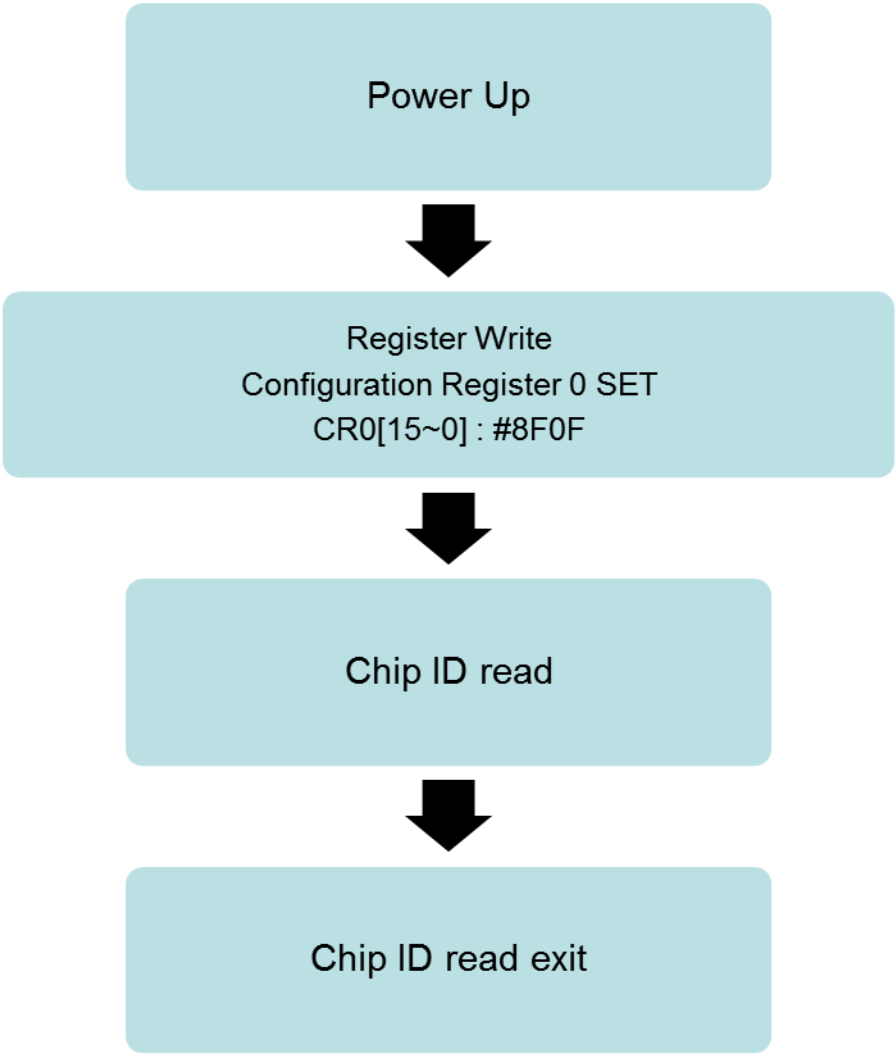
1. PREFACE

Winbond 64Mb HyperRAM is designed with a function called as Chip ID Read (CIDR) function for customer to identify the unique ID of each chip.

Further to the datasheet, this application note disclose the detail description of CIDR function for customer easy to use the function for purpose requested by specific application.

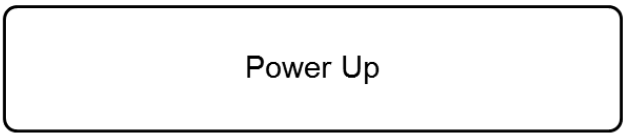
2. OPERATION SEQUENCE OF CHIP ID READ FUNCTION

CIDR function is able to be enabled as bleow sequence after power up.



2.1 Register Write:

The CIDR write sequence is set “configuration register 0 write” with OP code after power on. The “configuration register 0 write” is consisted by CA47~CA0, while controlling the state of all address pins as the OP code, data code is set as 8F0F after CA pin is set, Following is the CIDR enable sequence.



Command address :CA47~CA0

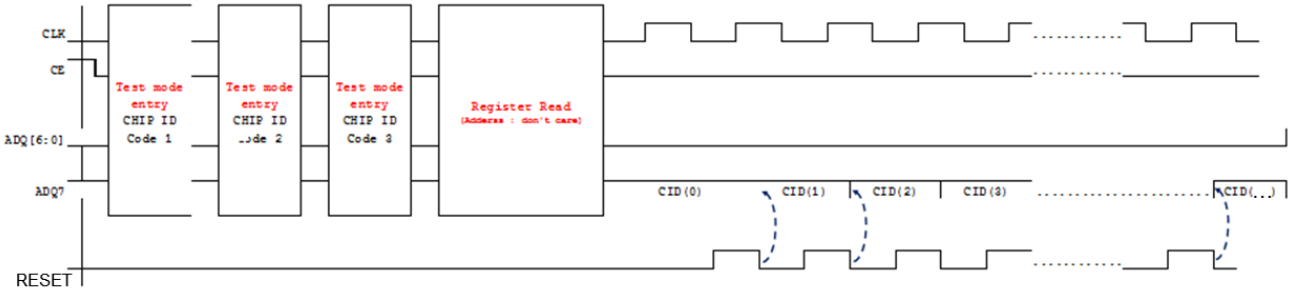
	CA					
	47~40	39~32	31~24	23~16	15~8	7~0
Configuration Register 0 Write	60h	00h	01h	00h	00h	00h

Data set :RG15~RG0

DQ	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
Code	8				F				0				F			

2.2 Chip ID read sequence:

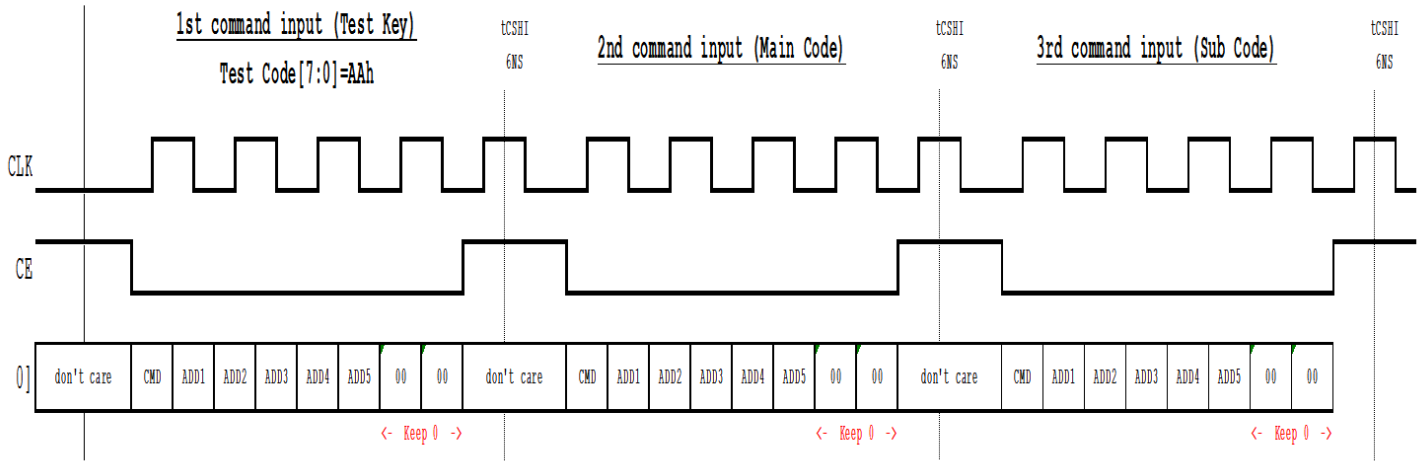
For the Chip ID read sequece, It must be executed by consecutive 3 chip ID code. Each chip ID code will execute 3 command input with 8 bit test code, Register read is execute after consecutive 3 chip ID code set finish, and chip ID will be readout at reset rising edge, while tCK must be bigger than 60ns, RESET=High > 30ns, RESET=Low > 30ns. Following is the Chip ID read sequence.



CHIP ID Code 1	1st command input: Test Key : Test Code[7:0]=AAh
	2nd command input: Main Code: Test Code[7:0]=00h
	3rd command input: Sub Code : Test Code[7:0]=00h
CHIP ID Code 2	1st command input: Test Key : Test Code[7:0]=AAh
	2nd command input: Main Code: Test Code[7:0]=27h
	3rd command input: Sub Code : Test Code[7:0]=20h
CHIP ID Code 3	1st command input: Test Key : Test Code[7:0]=AAh
	2nd command input: Main Code: Test Code[7:0]=09h
	3rd command input: Sub Code : Test Code[7:0]=10h

2.2.1 Test mode entry

Follow Chip ID read sequece, test mode is entry when each chip ID code is set. Each command input must write test code into both ADD2 and ADD3. Following is the Chip ID read sequence.



1st command input: Test Key = Test Code[7:0]=AAh
2nd command input: Main Code
3rd command input: Sub Code

CLK NO	Clock edge		ADQ							
CK-CK#			ADQ7	ADQ6	ADQ5	ADQ4	ADQ3	ADQ2	ADQ1	ADQ0
CK-CK#(N)	Rise	CMD	0	1	0	0	0	0	0	0
	Fall	ADD1	X	X	X	X	X	X	X	X
CK-CK#(N+1)	Rise	ADD2	Test Code[7]	Test Code[6]	Test Code[5]	Test Code[4]	X	1	X	0
	Fall	ADD3	Test Code[3]	Test Code[2]	Test Code[1]	Test Code[0]	X	X	X	X
CK-CK#(N+2)	Rise	ADD4	X	X	X	X	0	0	0	0
	Fall	ADD5	X	X	X	X	1	0	0	0

2.2.2 Register Read

Follow Chip ID read sequence, The “configuration register 0 (read)” must be set with OP code before chip ID readout. The “configuration register 0 (read)” is consisted by CA47~CA0, while controlling the state of all address pins as the OP code.
The chip ID read must be set 2 Latency count, Initial Latency count =5 clock ; Latency count1 + Latency count2 =10 clock.

	CA Bits					
Register	CA47~CA40	CA39~CA32	CA31~CA24	CA23~CA16	CA15~CA8	CA7~CA0
Configuration Register 0 (Read)	E0h	00h	01h	00h	00h	00h

2.2.3 Test mode exit

Test mode is exit after chip ID be readout, Following is the test mode exit code.

1st command input: Test Key : Test Code[7:0]=AAh
2nd command input: Main Code: Test Code[7:0]=56h
3rd command input: Sub Code : Test Code[7:0]=(Don’t care)

2.3 Chip ID decode

Following is the decode rule when chip ID be readout.

The valid chip ID code is CID[0] to CID[67], when chip ID code be readout after CID[68], they are don't care.

	CID(0)	CID(1)	CID(2)	CID(3)	CID(4)	CID(5)	CID(6)	CID(7)	CID(8)	CID(9)	CID(10)	CID(11)	CID(12)	CID(13)	CID(14)	CID(15)	CID(16)
	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Lot 1st						Lot 2nd				Lot 3rd			Lot 4th			
Decode table	ASCII						Binary				Binary			Binary			

CID(17)	CID(18)	CID(19)	CID(20)	CID(21)	CID(22)	CID(23)	CID(24)	CID(25)	CID(26)	CID(27)	CID(28)	CID(29)	CID(30)	CID(31)	CID(32)	CID(33)	CID(34)	CID(35)	CID(36)	CID(37)	CID(38)	CID(39)	CID(40)	CID(41)	CID(42)	CID(43)	CID(44)	CID(45)	CID(46)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Lot 5th						Lot 6th						Lot 7th						Lot 8th						Lot 9th					
ASCII						ASCII						ASCII						ASCII						ASCII					

CID(47)	CID(48)	CID(49)	CID(50)	CID(51)	CID(52)	CID(53)	CID(54)	CID(55)	CID(56)	CID(57)	CID(58)	CID(59)	CID(60)	CID(61)	CID(62)	CID(63)	CID(64)	CID(65)	CID(66)	CID(67)
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
wafer No.					X address (0~255)								Y address (0~255)							
Binary					Binary								Binary							

Code	ASCII	Code	ASCII	Code	ASCII
000000	0	001010	A	100100	a
000001	1	001011	B	100101	b
000010	2	001100	C	100110	c
000011	3	001101	D	100111	d
000100	4	001110	E	101000	e
000101	5	001111	F	101001	f
000110	6	010000	G	101010	g
000111	7	010001	H	101011	h
001000	8	010010	I	101100	i
001001	9	010011	J	101101	j
		010100	K	101110	k
		010101	L	101111	l
		010110	M	110000	m
		010111	N	110001	n
		011000	O	110010	o
		011001	P	110011	p
		011010	Q	110100	q
		011011	R	110101	r
		011100	S	110110	s
		011101	T	110111	t
		011110	U	111000	u
		011111	V	111001	v
		100000	W	111010	w
		100001	X	111011	x
		100010	Y	111100	y
		100011	Z	111101	z

Code	Binary
00000	0
00001	1
00010	2
00011	3
00100	4
00101	5
00110	6
00111	7
01000	8
01001	9
01010	10
01011	11
01100	12
.....	.....
10100	20
10101	21
10110	22
10111	23
11000	24
11001	25
11010	26
11011	27
11100	28
11101	29
11110	30
11111	31
.....	.....

3. MEASUREMENT OF CHIP ID READ SEQUENCE BY MOSAID TESTER

The CHIP ID is correctly readout under below conditions.

	Measurement 1
tCK	60ns (16Mhz)
Chip ID Readout result	DUT 1: LOT:6944453BK WAFER: 18 ESI: (081, 025) DUT 2: LOT:6944453BK WAFER: 18 ESI: (157, 025) DUT 3: LOT:6944453BK WAFER: 18 ESI: (114, 021) DUT 4: LOT:6944453BK WAFER: 18 ESI: (124, 011)

4. REVISION HISTORY

Revision	Date	Page	Description
P01	2021/8/13	All	Initial created